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JAN 78 G L VARNELL, R A WILLIAMSON, T BREWER DAAB07-76-C-8105
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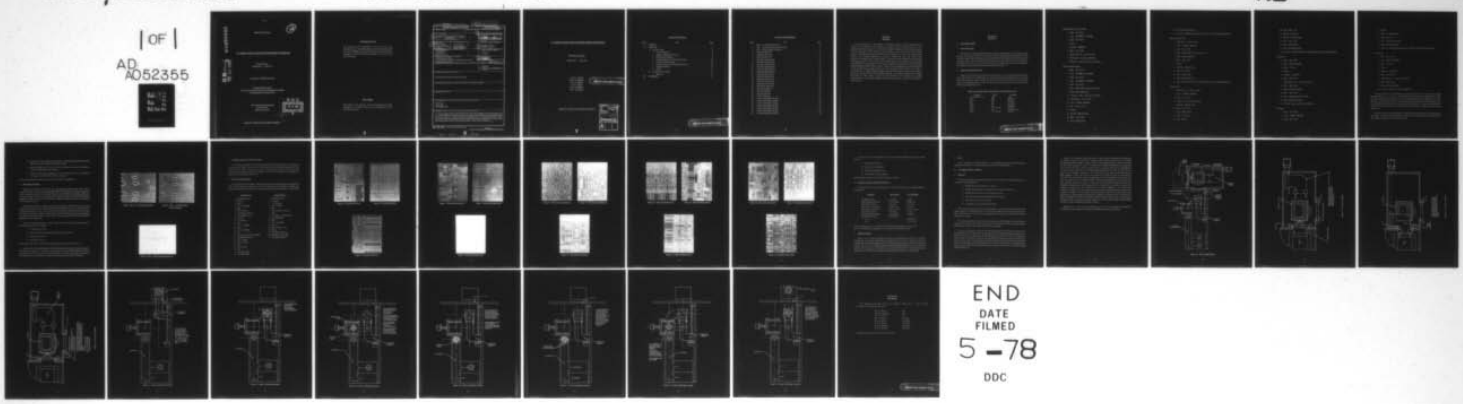

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Third Quarterly Report

IC FABRICATION USING ELECTRON-BEAM TECHNOLOGY

Period Covered
1 March 1977 – 1 June 1977

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Technical Support Activity
U.S. Army Electronics Research and Development Command
Fort Monmouth, New Jersey 07703

Texas Instruments Incorporated
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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

Slice processing and process development on the 256-bit bipolar RAMs has continued this quarter. Four lots of bipolar RAMs are presently in process and the oxidation, epitaxial and diffusion parameters from these lots have been measured. A comparison between the measured parameters and their specified values has been made. The processes from polished substrate through DUF O.R. have been significantly modified to reduce cost and processing steps. Work on improving the alignment marker process is continuing.

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IC FABRICATION USING ELECTRON-BEAM TECHNOLOGY

Third Quarterly Report

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SECTION I
PURPOSE

The overall objective of the program is to implement e-beam writing technology for the fabrication of microcircuits. The technical and economic impact of electron-beam direct slice printing will be demonstrated on 256-bit bipolar RAMs. The elimination of mask masters, masks, and the masking process will eliminate the most significant source of yield loss. This will permit greater circuit design complexity and flexibility which will lead to lower device costs with increased reliability. The complete implementation program is divided into three tasks. Task A, Yield Improvement Through Direct E-Beam Writing, is directed toward developing the manufacturing technology required for e-beam writing with existing equipment and existing resist processes and demonstrating the yield benefits of this technique. Task B, Cost Reduction for E-Beam Writing Through High Speed Resist Implementation, is directed toward implementing identified high speed e-beam resists in order to significantly decrease cycle time and thus reduce the IC bar cost. Task C, Cost Reduction for E-Beam Writing Through Automatic Beam Diameter Control and Automatic Handling, is directed toward utilizing EBMIII's capability of computer-controlled beam size (large and small) on high density circuit ($\leq$0.1 mil) geometries. This program also included implementation of an automated handling system for slices to reduce cycle time and thus further reduce bar cost.

SECTION II
RESULTS

A. SLICE PROCESSING

1. General Discussion

Fabrication of 256-bit bipolar RAMs has required the modification of many existing e-beam processes. The pattern distortion from epitaxial growth required significant modification of the alignment marker system. Simultaneously etching different oxide thicknesses such as at the emitter and contact O.R. steps has sometimes caused staining of the oxide windows. The processes listed in the subsequent text represent a refinement of basic e-beam lithographic processes to accommodate the stringent requirements of high density bipolar RAM processing.

2. E-Beam Lithographic Processes

Table I lists the process step, resist and etch process for each level in the fabrication process. The actual specifics of each lithographic step, such as spin speeds, bake temperatures, etc., are listed below. The alignment markers through contact O.R. processes have been used on the material in process. The remaining processes have been verified on test slices and they will be used when the lots in process reach those steps.

Table I. Process Step, Resist, and Etch Process for Fabrication Level

Process Step	Resist	Etch Process
Alignment Markers I and II	PMMA	Plasma
DUF	PBS	Buffered HF
Isolation	PBS	Buffered HF
Base	PBS	Buffered HF
Emitter	PBS	Buffered HF
Contact	PBS	Buffered HF
Leads I	TI resist No. 309	Metex Etch
Vias	PBS	Ethylene Glycol/HF
Leads II	TI resist No. 309	Metex Etch

Alignment Markers I and II Steps

1. Bake – IR @ 160°C
2. Coat – 8% PMMA @ 1.5K RPM
3. Bake – IR @ 160°C
4. Expose
5. Develop – MIBK/IPA
6. Bake – IR @ 160°C
7. Plasma De-scum – O_2 @ 100 watts
8. Plasma etch – CF_4/O_2 @ 300 watts
9. Clean-up – Plasma, 10 min O_2 @ 300 watts

DUF and Isolation Steps

1. Bake – IR @ 160°C
2. Coat – 8% PMMA @ 1.5K RPM
3. Bake – IR @ 160°C
4. Coat – 8% PMMA @ 1.5K RPM
5. Bake – IR @ 160°C
6. Etch – Buffered HF until back side clears
7. Rinse and Spin Rinse/Dry
8. Clean-up – Asher, 15 min O_2 @ 300 watts
9. Steam slices – 5 min @ 700°C
10. Coat – 5% PBS @ 2K RPM
11. Bake – IR @ 120°C
12. Expose
13. Develop – PBS Developer
14. Bake – IR @ 120°C
15. Etch – Buffered HF

16. Rinse and Spin Rinse/Dry
17. Clean-up – Methyl Ethyl Ketone Strip, IPA rinse, D.I. H_2O, Spin Rinse/Dry

Base and Emitter Steps

1. Steam Slices – 5 min @ 700°C
2. Coat – 5% PBS @ 2K RPM
3. Bake – IR @ 120°C
4. Etch – Buffered HF until back side clears
5. Rinse and Spin Rinse/Dry
6. Bake – IR @ 120°C
7. Expose
8. Develop – PBS Developer
9. Bake – IR @ 120°C
10. Etch – Buffered HF
11. Rinse and Spin Rinse/Dry
12. Clean-up – Methyl Ethyl Ketone Strip, IPA Rinse, D.I. H_2O, Spin Rinse/Dry

Contact Steps

1. N_2 bake slices – 30 min @ 700°C
2. Coat – 5% PBS @ 2K RPM
3. Bake – IR @ 120°C
4. Expose – P-Contacts and Schottky
5. Develop – PBS Developer
6. Bake – IR @ 120°C
7. Etch – Buffered HF
8. Rinse – D.I. H_2O
9. Dry – N_2 Box

10. Bake – IR @ 120°C
11. Expose – N-Contacts
12. Develop – PBS Developer
13. Bake – IR @ 120°C
14. Etch – Buffered HF
15. Rinse and Spin Rinse/Dry
16. Clean-up – Methyl Ethyl Ketone Strip, IPA rinse, D.I. H_2O, Spin Rinse/Dry

Leads I Step

1. Bake – IR @ 160°C
2. Coat – TI309 @ 2K RPM
3. Bake – 50°C Air
4. Expose
5. Develop – Xylene/IPA
6. Bake – IR @ 160°C
7. Plasma De-scum – 2 min O_2 @ 100 watts
8. Etch – Metex Etch
9. Rinse and Spin Rinse/Dry
10. Bake – IR @ 120°C
11. Etch – Hydrogen Peroxide @ 30°C
12. Rinse and Spin Rinse/Dry
13. Clean-up – Plasma, 10 min O_2 @ 300 watts

Vias Step

1. Bake – IR @ 160°C
2. Coat – 5% PBS @ 2K RPM
3. Bake – IR @ 120°C

4. Expose
5. Develop – PBS Developer
6. Bake – IR @ 120°C
7. Etch – Ethylene Glycol/HF
8. Rinse and Spin Rinse/Dry
9. Clean-up – Methyl Ethyl Ketone Strip, IPA Rinse, D.I. H_2O, Spin Rinse/Dry

Leads II Step

1. Bake – IR @ 160°C
2. Coat – TI309 @ 2K RPM
3. Bake – 50°C Air
4. Expose
5. Develop – Xylene/IPA
6. Bake – IR @ 160°C
7. Plasma De-scum – 2 min O_2 @ 100 watts
8. Etch – Metex Etch
9. Rinse and Spin Rinse/Dry
10. Clean-up – Plasma, 10 min O_2 @ 300 watts

It should be clear from examination of the processes that they are quite similar to regular photoresist processes. In fact they are almost identical. The electron resist is applied to slices using the same equipment and techniques as is used to apply photoresist: resist is dispensed on the slices and they are spun until dry. The bake ovens are IR heated and the slices proceed through the oven on a belt below the IR lamps. After exposure, the slices are placed on a spray developer and spun while the developer is sprayed on the slices. Again these processes are identical to those used on photoresist.

Not only are the electron-beam processes similar to photoresist processes, their problems are also similar. A number of these problems are discussed in the PBS Adhesion Problems section. Several general precautions that should be taken are:

1) Control the room humidity and temperature. If the humidity gets much below 30%, PBS does not adhere well and its sensitivity changes.

2) Keep air bubbles out of the resist. If this is not done, the resist goes on the slices in streaks, and the pinhole count increases.

3) Control the IR bake temperatures. If the temperatures get too hot, PBS will decompose and TI309 will flow off the oxide steps.

If the previously mentioned precautions are taken, the results are usually good.

3. PBS Adhesion Problems

PBS does not adhere to oxide surfaces very well, especially phosphorus glass oxides, without special treatments to the slices before applying the PBS. Normally slices see a nitrogen ambient just prior to being removed from the furnace tube. However unless the PBS is immediately applied upon their removal from the furnace, severe undercutting will result at the subsequent O.R. Immediate application of PBS is usually not feasible because of logistics problems so we have had to proceed by two alternative routes.

The routine procedure is to give the slices a low temperature ($\approx 700°C$) treatment in a steam ambient for 5 minutes prior to applying the PBS. This procedure works quite well but also has several problems. One is that it is an extra process step which increases cycle time and slice processing cost. Second, it cannot be used prior to Contact O.R. because of its affects on transistor h_{FE}s at low temperatures and low currents. Third, it cannot be used at Vias because the slices have aluminum on them at this point.

The other alternative procedure is to apply a silane film to the slices prior to the application of PBS. This procedure is done as follows:

1) IR bake slices at 160°C

2) Spin 2% Phenyltrichlorosilane (PTCS) in Xylene on the slices

3) IR bake slices at 160°C

4) Spin PBS on the slices

This procedure has worked well and it is presently being used at Contact O.R. and Vias.

Included are some photographs taken from blank oxidized slices that were patterned using the previous three procedures: no treatment, low temperature steam, and PTCS application. Figure 1 was taken from a slice that received no treatments, Figure 2 was taken from a slice that received a low temperature steam, and Figure 3 was taken from a slice that received a PTCS treatment.

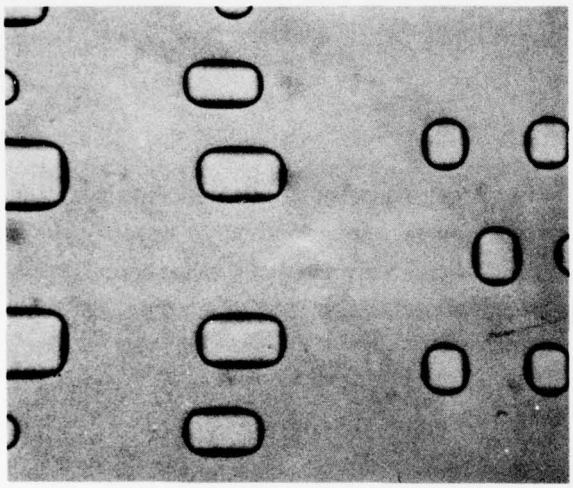

Figure 1. Slice – No Treatment Procedure

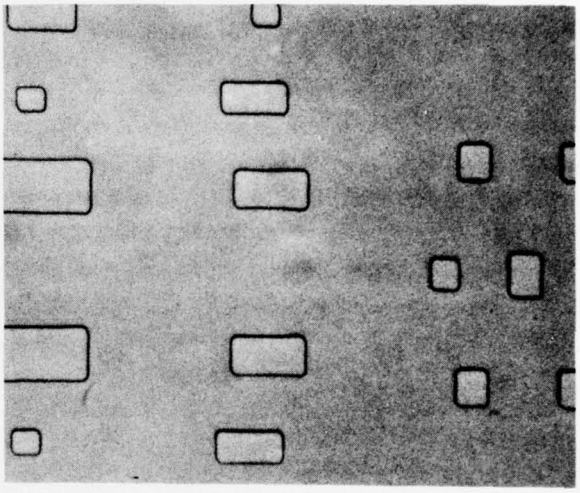

Figure 2. Slice – Low Temperature Steam Procedure

Figure 3. Slice – PTCS Treatment Procedure

4. Chip Photographs at Various Process Steps

The following photographs, taken at various steps in the fabrication process, are representative of the overall slice quality seen on all of the lots processed to date. Figures 4 through 6 were taken after DUF O.R., Figures 7 through 9 were taken after Isolation O.R., Figures 10 through 12 were taken after Base Diffusion, Figures 13 through 15 were taken after Emitter O.R., and Figures 16 through 18 were taken after Contact O.R.

5. New Process Development

At the present time the number of steps required to process a polished substrate through DUF O.R. is quite considerable. Therefore on Lot 4 our procedures were modified to simplify these processes. A step-by-step comparison of the present process and the proposed process is presented.

Present Process

1. Polished Substrate
2. Clean-up
3. Bake
4. Coat with PMMA
5. Bake
6. Pattern Markers
7. Etch Markers (Plasma)
8. Strip PMMA (Plasma)
9. Clean-up
10. 1st Oxidation
11. Bake
12. Coat with PMMA
13. Bake
14. Coat with PMMA
15. Bake
16. Strip oxide from back side (HF)
17. Strip PMMA (Plasma)
18. 700°C Steam
19. Coat with PBS
20. Bake
21. Pattern DUF
22. Bake
23. Etch Oxide (HF)
24. Strip PBS (MEK)

Proposed Process

1. Polished Substrate
2. Clean-up
3. 1st Oxidation
4. Coat with PBS
5. Bake
6. Pattern Markers and DUF
7. Bake
8. Etch Markers and DUF (HF)
9. Strip PBS (MEK)
10. Bake
11. Coat with PMMA
12. Bake
13. Pattern Marker Covers
14. Bake
15. Etch Markers (Plasma)
16. Etch Marker Covers (HF)
17. Strip PMMA (Plasma)

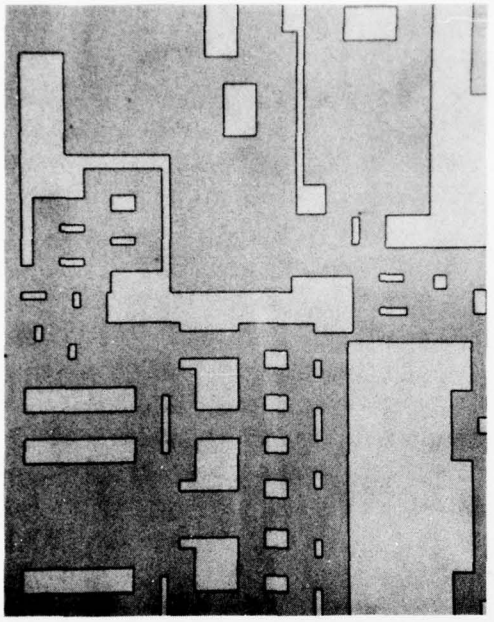

Figure 4. Chip After DUF O.R.

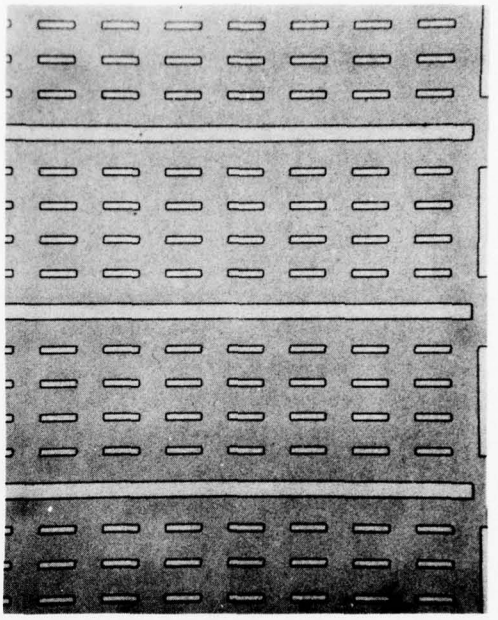

Figure 5. Chip After DUF O.R.

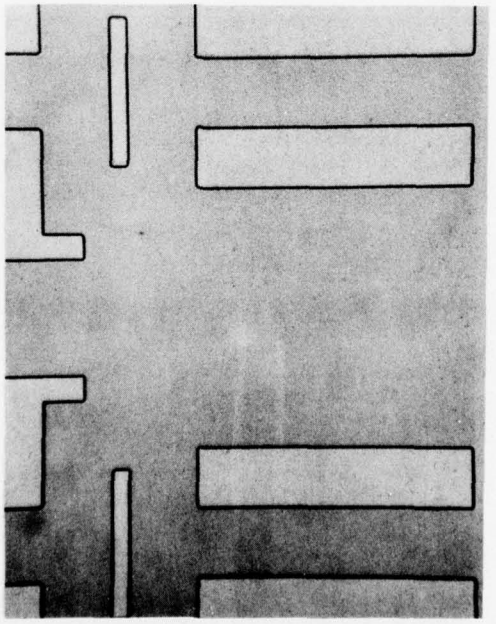

Figure 6. Chip After DUF O.R.

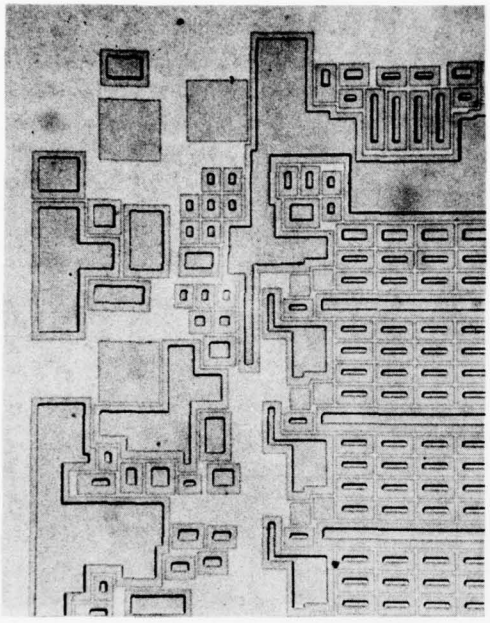

Figure 7. Chip After Isolation O.R.

Figure 8. Chip After Isolation O.R.

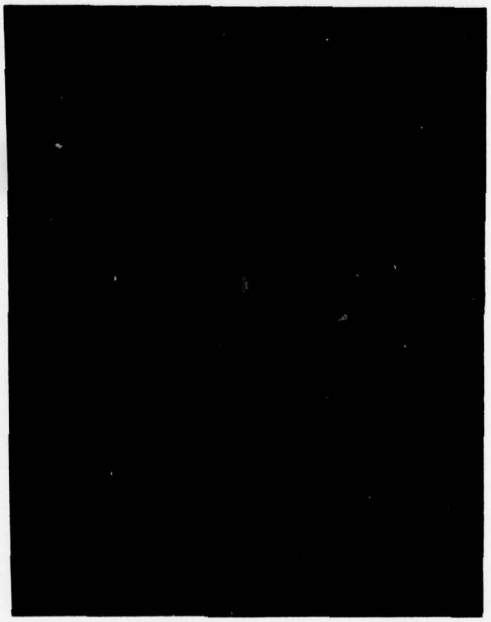

Figure 9. Chip After Isolation O.R.

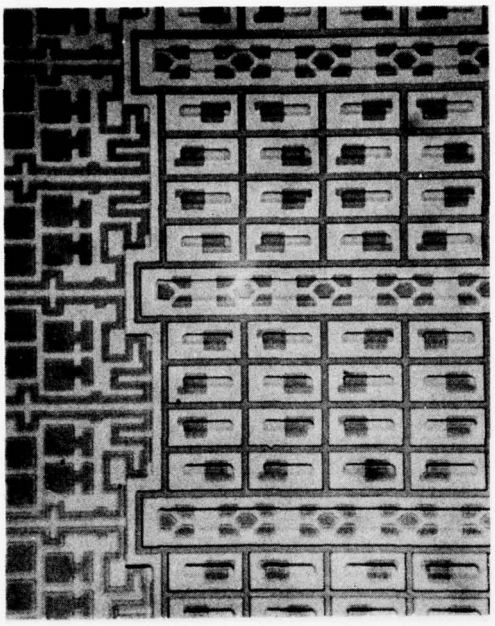

Figure 10. Chip After Base Diffusion

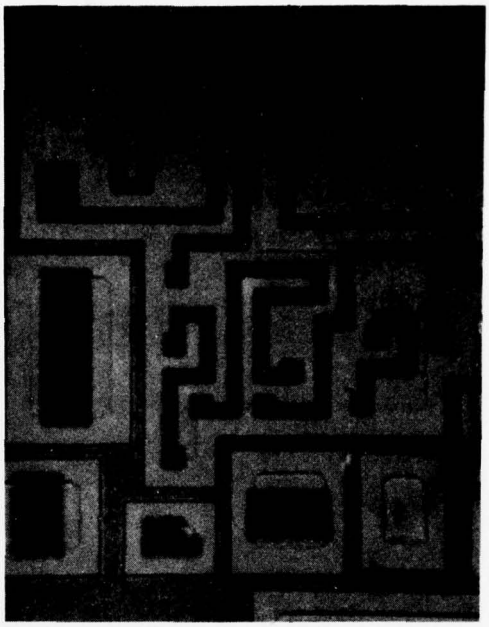

Figure 11. Chip After Base Diffusion

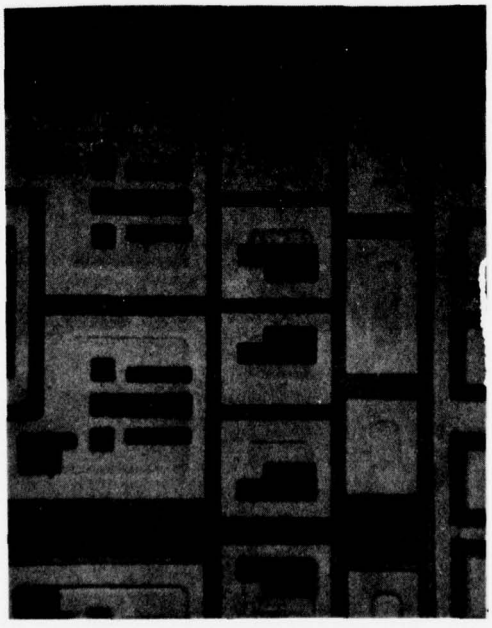

Figure 12. Chip After Base Diffusion

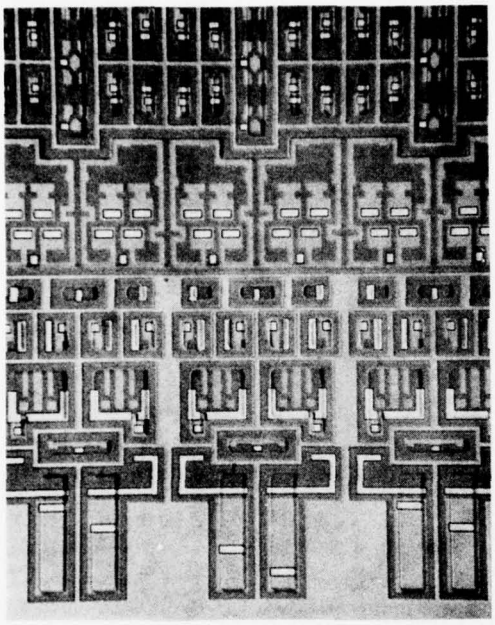

Figure 13. Chip After Emitter O.R.

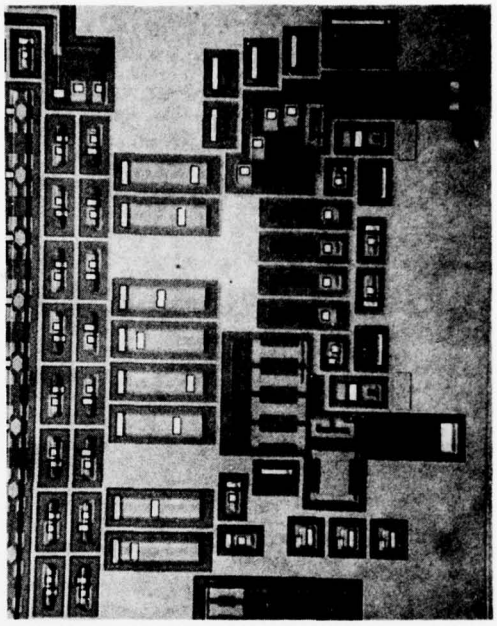

Figure 14. Chip After Emitter O.R.

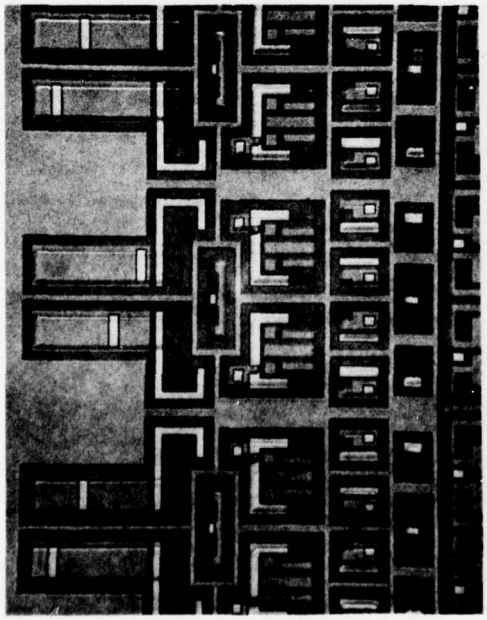

Figure 15. Chip After Emitter O.R.

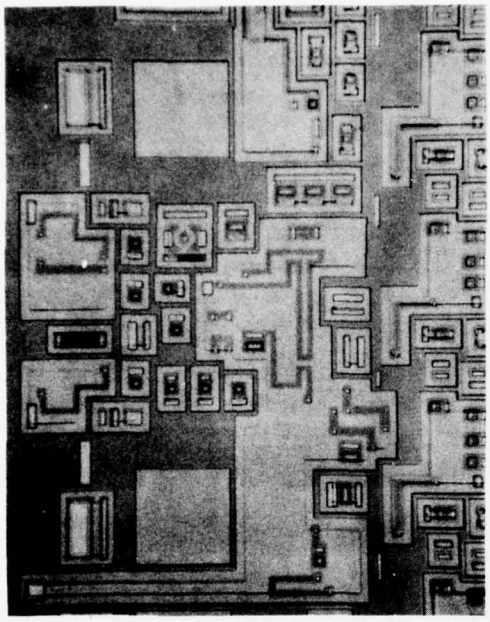

Figure 16. Chip After Contact O.R.

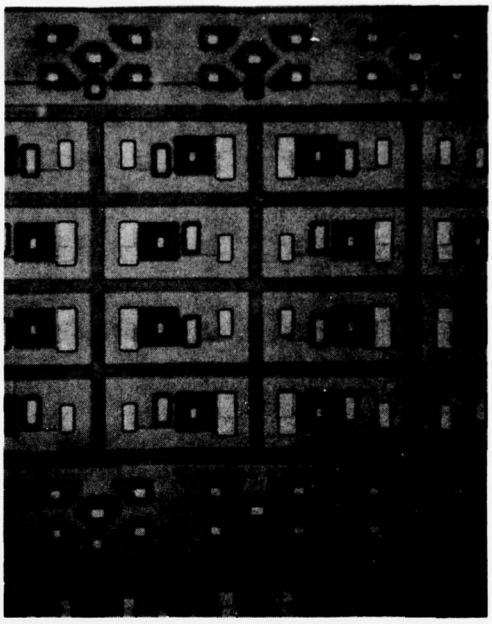

Figure 17. Chip After Contact O.R.

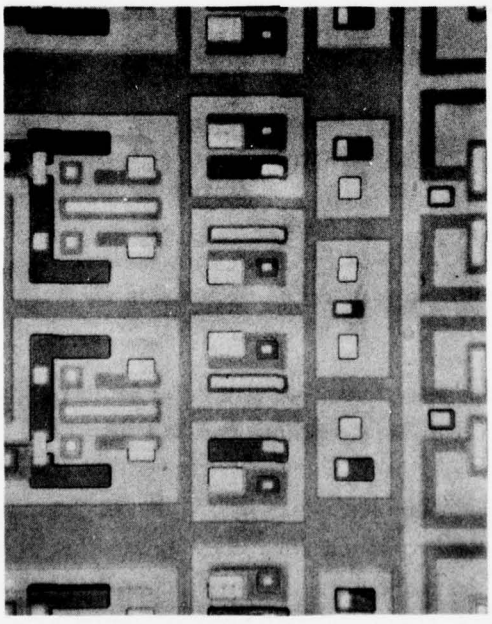

Figure 18. Chip After Contact O.R.

As can be seen from the comparison, there are several major advantages to the new procedure. They are:

1) Seven less process steps

2) One less furnace operation

3) One less slice alignment step

4) Perfect DUF to marker alignment

This procedure was used on Lot 4 which is presently in process.

6. Oxidation, Epitaxial and Diffusion Parameters

Listed below are the actual readings taken from the lots in process as compared against the specifications.

Parameter	Specification	Actual Reading
1st Oxide Thickness	8.5-9.5 KÅ	9.2 KÅ
DUF Diffusion Depth (Xj)	35-45 Hg lines	44 Hg lines
DUF Diffusion Sheet	14-18 Ω/□	10-12 Ω/□
Epitaxial Layer Thickness	0.10-0.12 mil	0.12 mil
Epitaxial Layer Resistivity	0.28-0.32 Ω-cm	0.27-0.30 Ω-cm
2nd Oxide Thickness	4.8-5.4 KÅ	5.2 KÅ
Isolation Diffusion Depth	10-12 Hg lines	10 Hg lines
Base Diffusion Sheet	180-220 Ω/□	
Lot 1		240-260 Ω/□
Lot 2		193-202 Ω/□

All of the readings are close to being within specification except the base diffusion sheet on Lot 1. This high sheet reading may make these devices fail electrical testing.

7. Alignment Markers

Because of the pattern distortion caused by the epitaxial growth process, it has been impossible to automatically align Markers II to Marker I on Lots 2 and 3. Therefore, they were manually aligned. During this alignment, some offset and gain was introduced into the second set of markers. This, of course, is repeated with each subsequent alignment. However, it is not a serious problem and all programs were changed to accommodate this deviation. The offset error was approximately 0.10 mil and the gain error was approximately 0.20 mil over a 200-mil field.

8. Status

Lot 1 is presently at first-level metal; Lot 2 was scrapped because the wrong base diffusion temperature was used; Lot 3 is at base diffusion; and Lot 4 is at DUF diffusion.

B. AUTOMATIC SLICE LOADING

1. Approach

The various constraints and requirements placed on an automatic slice handling system for an e-beam slice printing machine are:

1) Aligning the slice flat to within ±1/2 degree
2) Positioning the slice surface accurately in the focal plane of the beam
3) Reliable electrical contact to the backside of the slice
4) No mechanical vibration produced during slice exposure
5) 60 seconds or less vacuum cycle time
6) Compatibility with existing machine designs

The first three requirements were the most difficult to achieve. TI has been successful in the design, fabrication and implementation of an optical flat aligner capable of the required accuracy. Only a small amount of redesign of this existing prealigner was necessary to adapt it to the purpose described in this work.

The second requirement will be achieved by utilizing a "double banking" slice holder design in which the slice surface is first referenced to a surface inside the slice holder and the slice holder is then banked to a fixed reference plane inside the vacuum chamber.

Contact to the backside of the slice will be made via capacitive discharge forming circuit. A large capacitor is first charged with a power supply and then discharged through contacts to the backside of the slice to break down any SiO_2 present on the back of the slice. The contacts can then be tested via an ohmmeter circuit at any time during the exposure and can be reformed at any time if necessary. The contact points are part of the slice holder and contact forming and testing are done after final alignment and z-banking inside the exposed vacuum chamber. A prototype of this circuit has been built and tested and allows good reproducible contacts to be formed through 10,000 Å SiO_2 layers.

Figure 19 is a drawing of the loading system. A cassette load of unexposed slices is placed in the unloader at point A. A single slice is unloaded and transported down the air track to point B and the flat located to within ±1/2 degree. The slice is then clamped into a slice holder, and rotated 90° into the B′ load position. Valve V_1 is opened and the holder is shuttled into the vacuum lock. First the outer valve (V_1) is closed, the inner valve (V_2) is opened, and vacuum is reestablished in the air lock. The exposed slice in the E-Beam Machine Stage (C) is moved to the lower elevator pocket by the Fork Slide Assembly (2). The elevator moves to the bottom position and the Fork Slide Assembly (2) moves the new slice (in carrier) to the Stage (C) from the upper elevator pocket (D). The inner valve (V_2) closes, nitrogen fills the air lock to atmospheric pressure, the outer valve (V_1) opens and the Fork Slide Assembly (1) places an incoming slice (in a carrier) into the upper elevator pocket. The elevator is raised and the Fork Slide Assembly (1) removes the completed slice from the lower elevator pocket. The outer valve (V_1) closes and the vacuum lock chamber is pumped down. The completed slice is rotated 90 degrees by the transfer from position B′ to B. The slice is then unclamped from the carrier and loaded on the air track where it proceeds to position E. In this manner, an unexposed slice is always in the vacuum lock being outgassed by vacuum pumping while awaiting the completion of the previous slice. Continuous slice flow is maintained and nearly all overhead associated with slice transport and vacuum cycling is eliminated. There is a physical separation between the Vacuum Lock Assembly and the Prealign Assembly to permit prealignment during slice writing.

Figures 20, 21, and 22 show the operation of the Air Lock Assembly and Figures 23 through 29 show the operation of the loader and Prealign Assembly in greater detail.

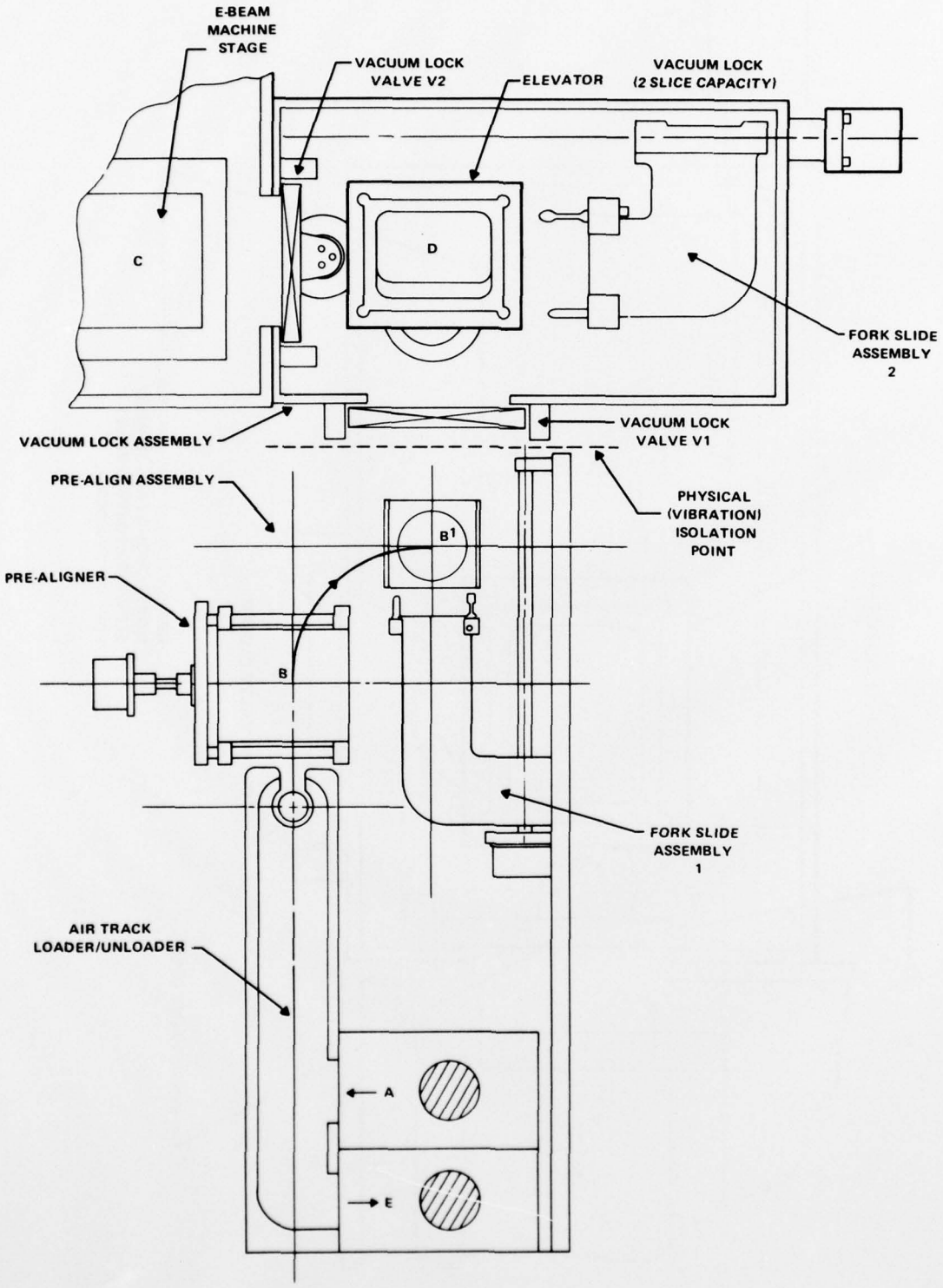

Figure 19. Slice Loading System

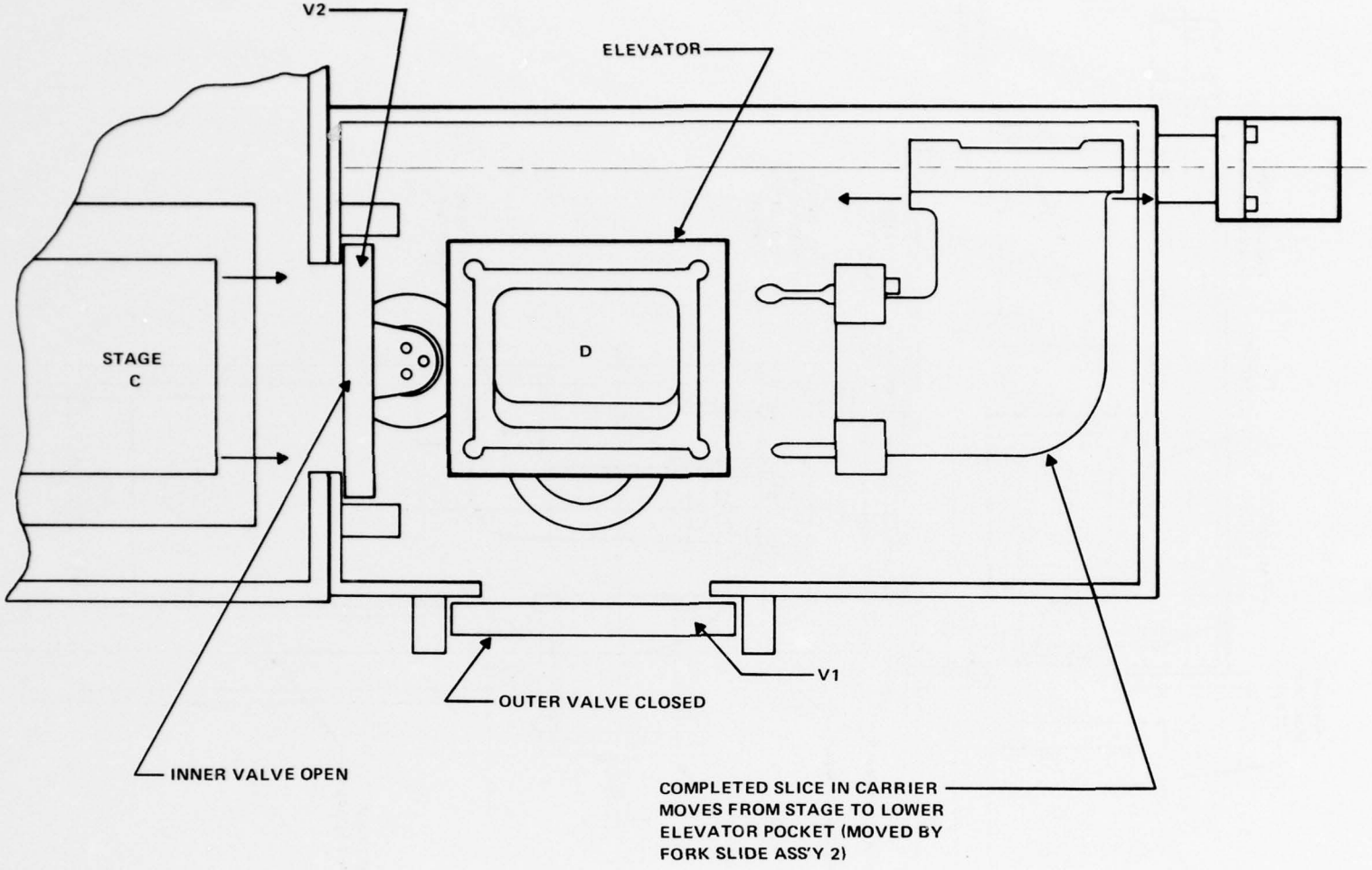

Figure 20. Air Lock Assembly

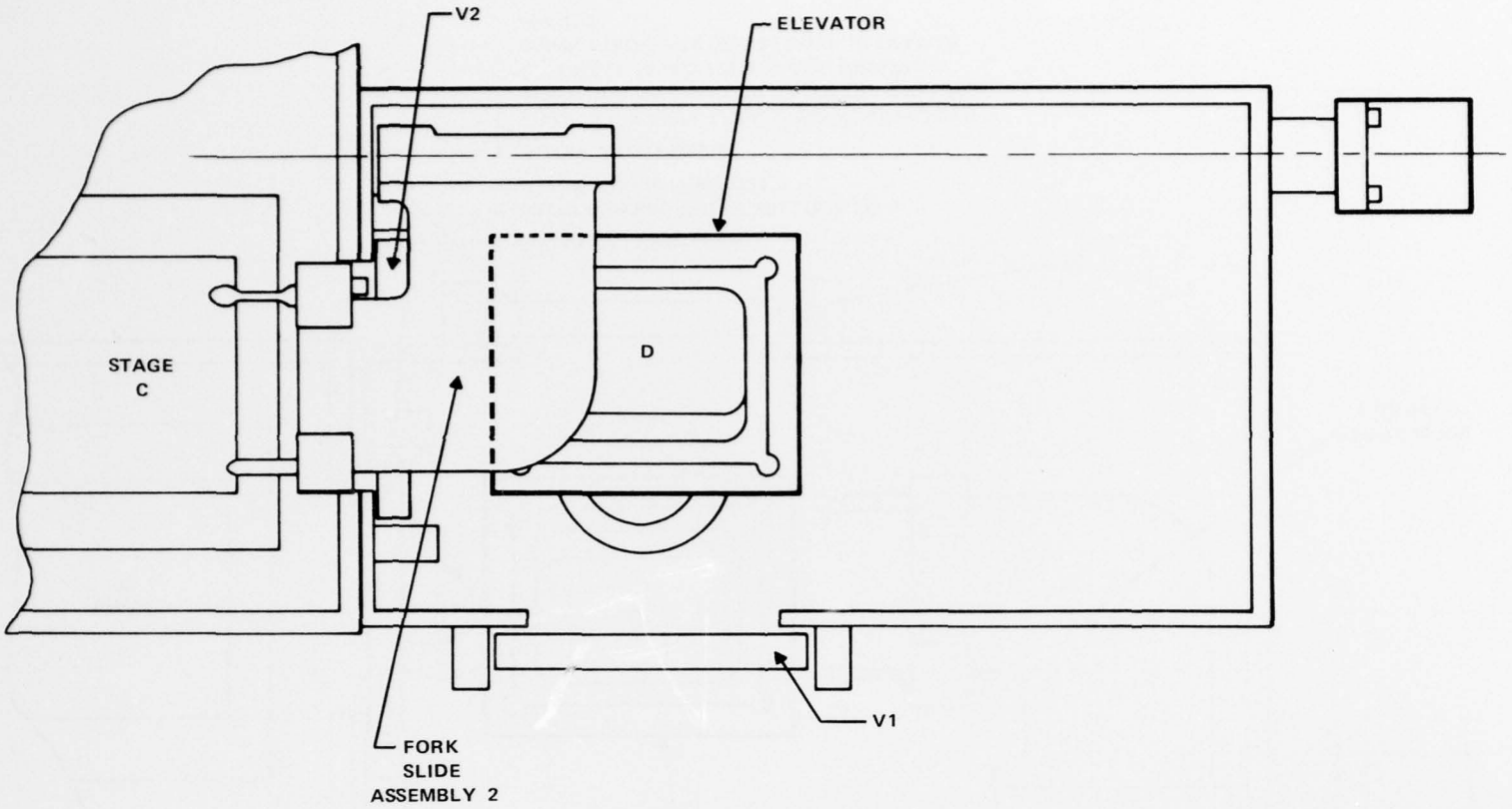

Figure 21. Air Lock Assembly

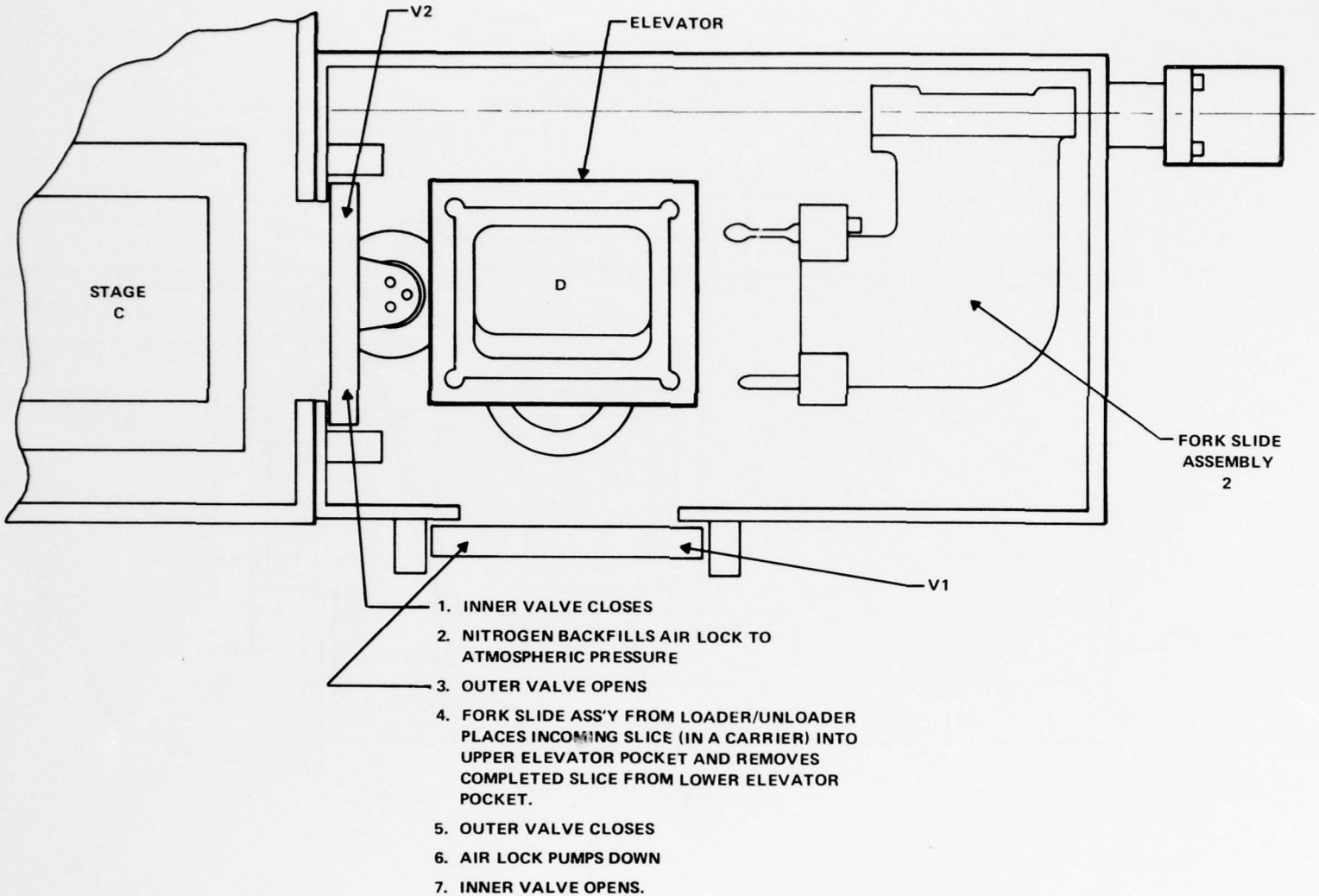

Figure 22. Air Lock Assembly

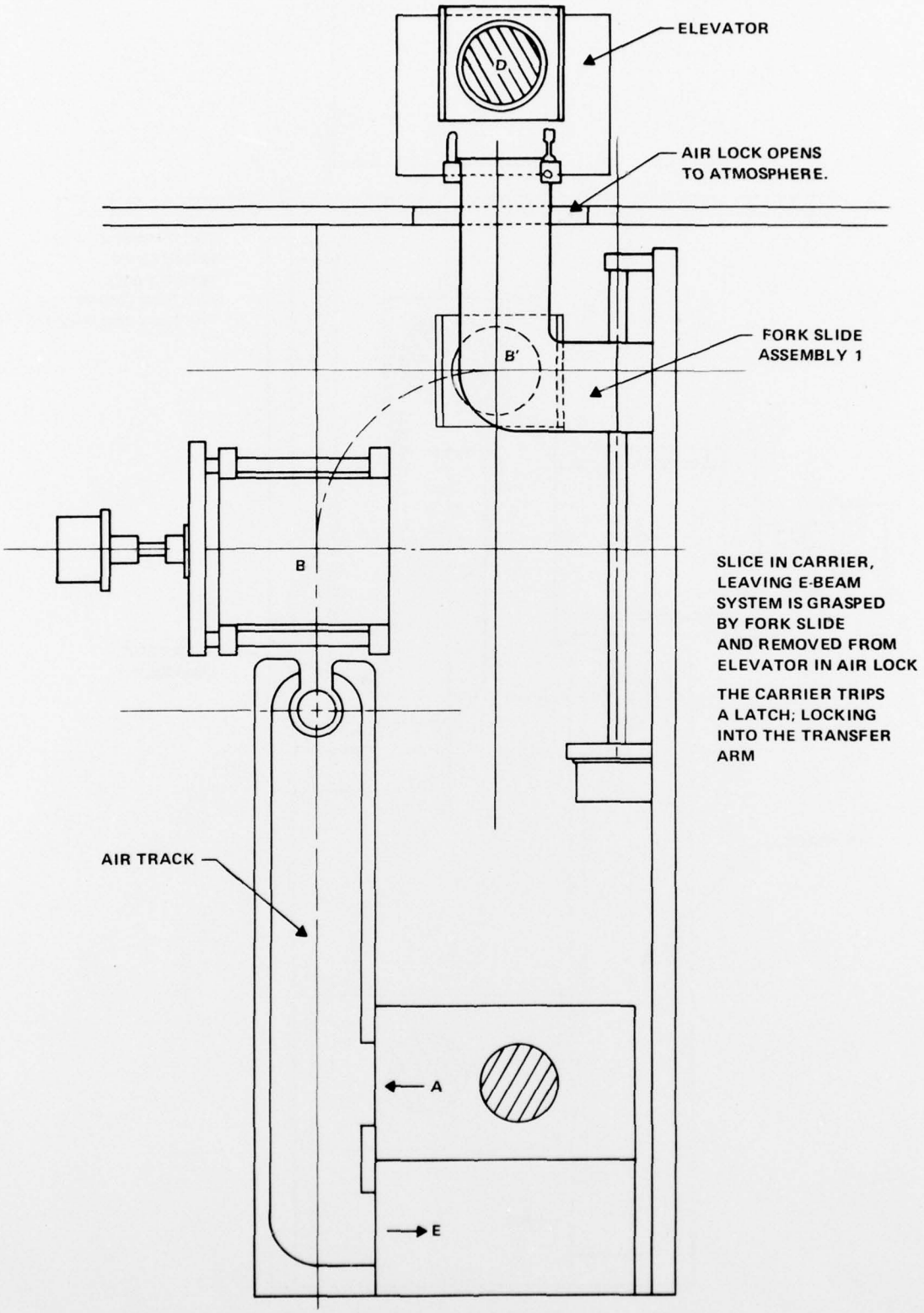

Figure 23. Loader and Prealign Assembly

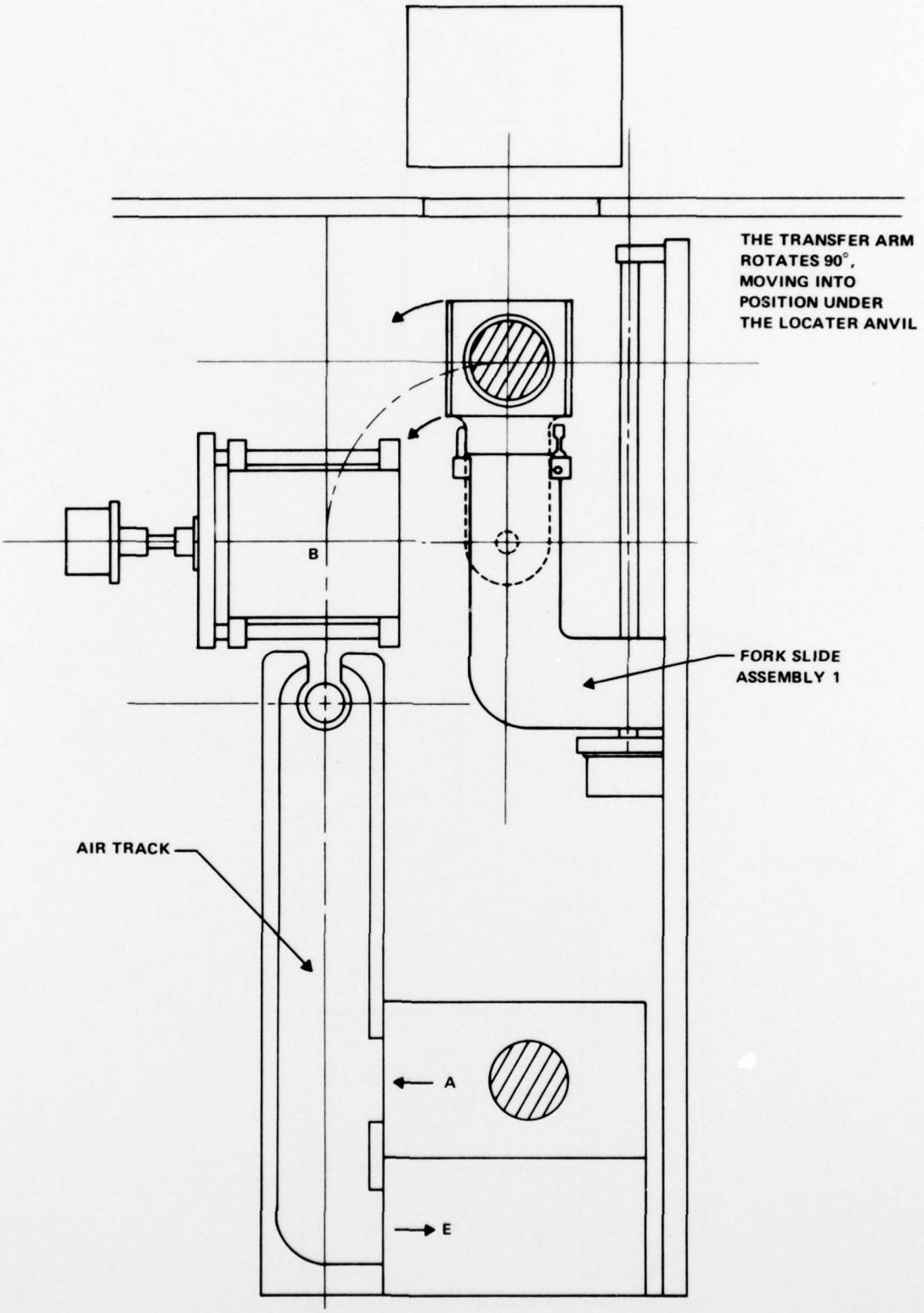

Figure 24. Loader and Prealign Assembly

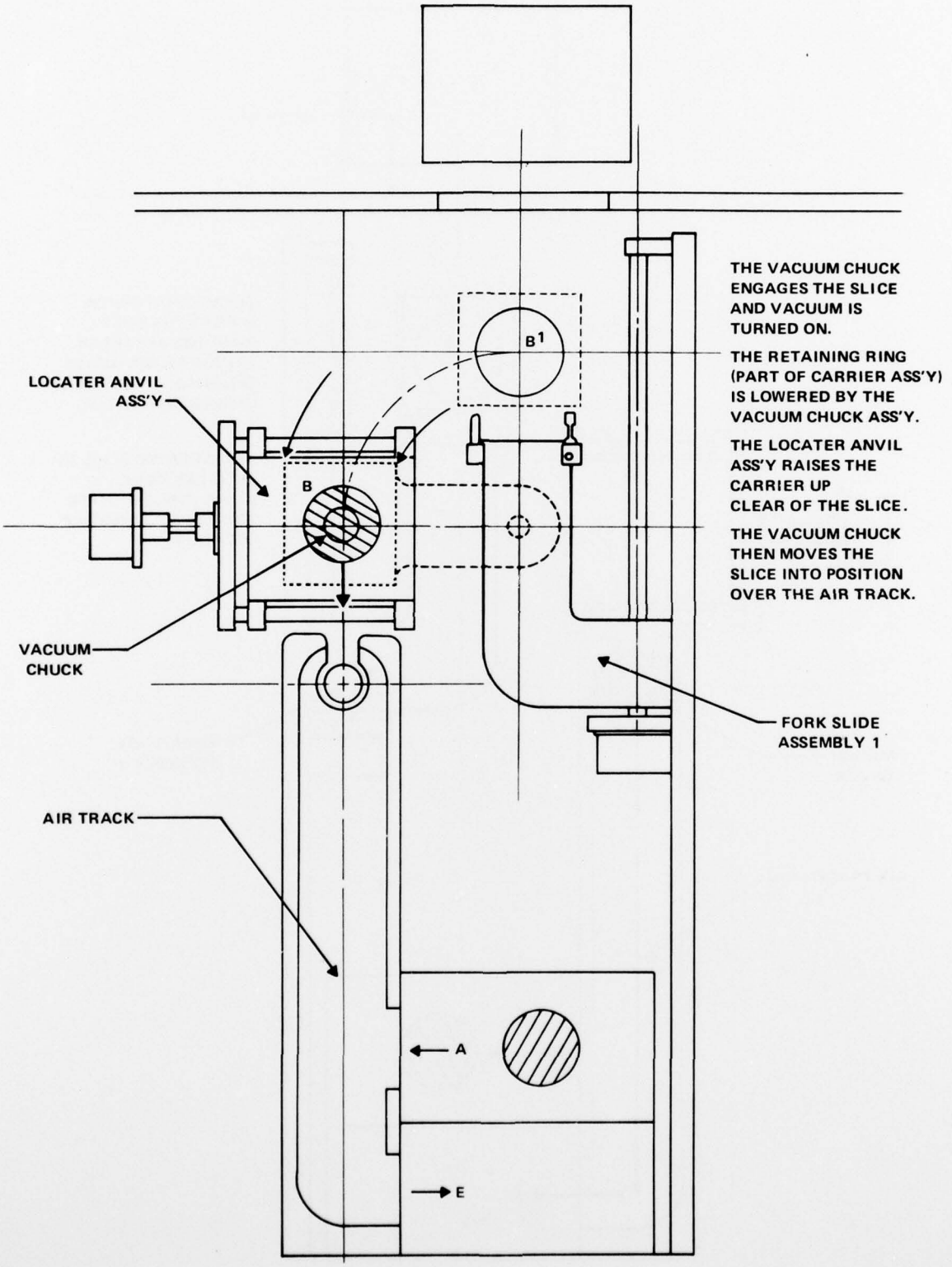

Figure 25. Loader and Prealign Assembly

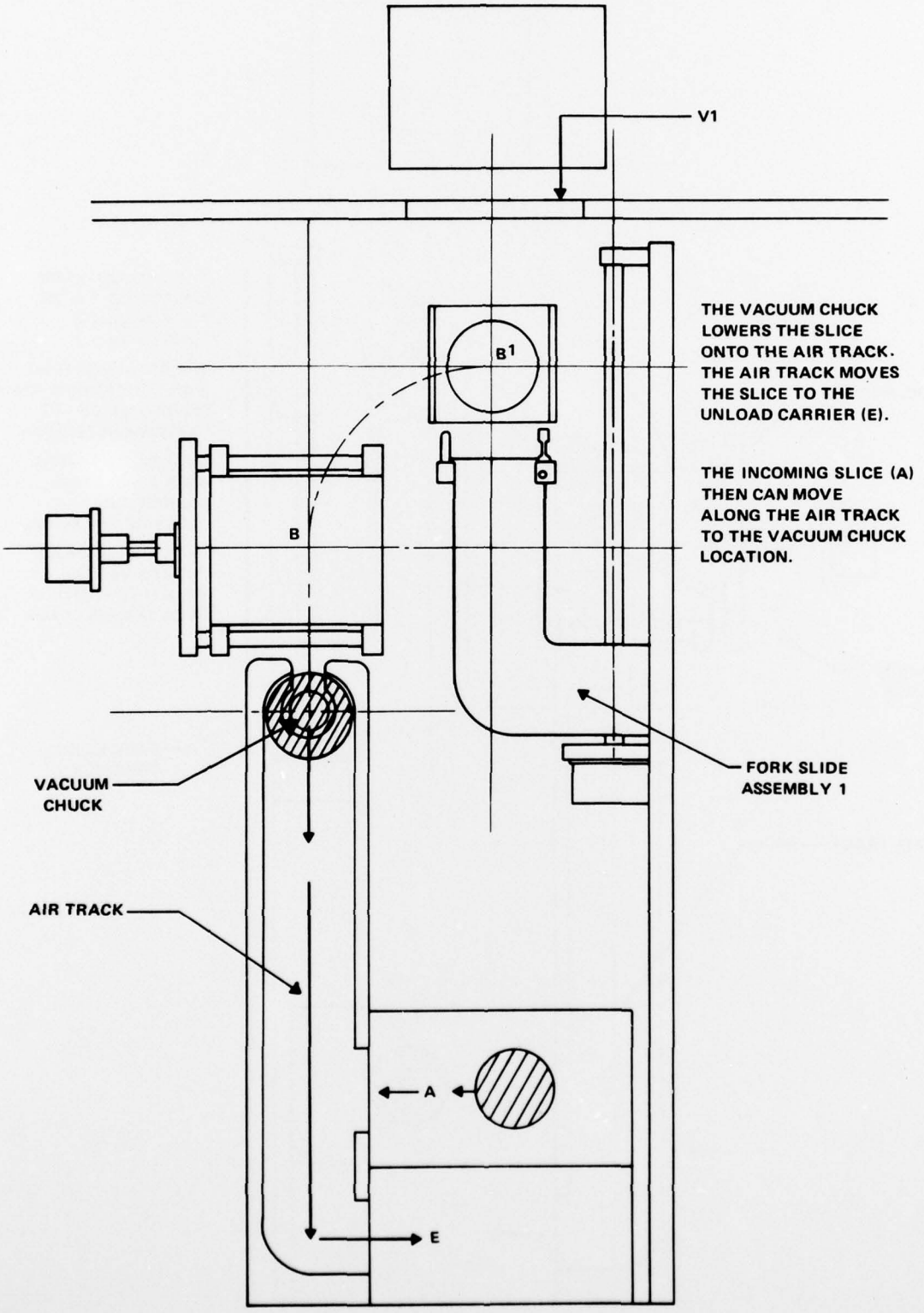

Figure 26. Loader and Prealign Assembly

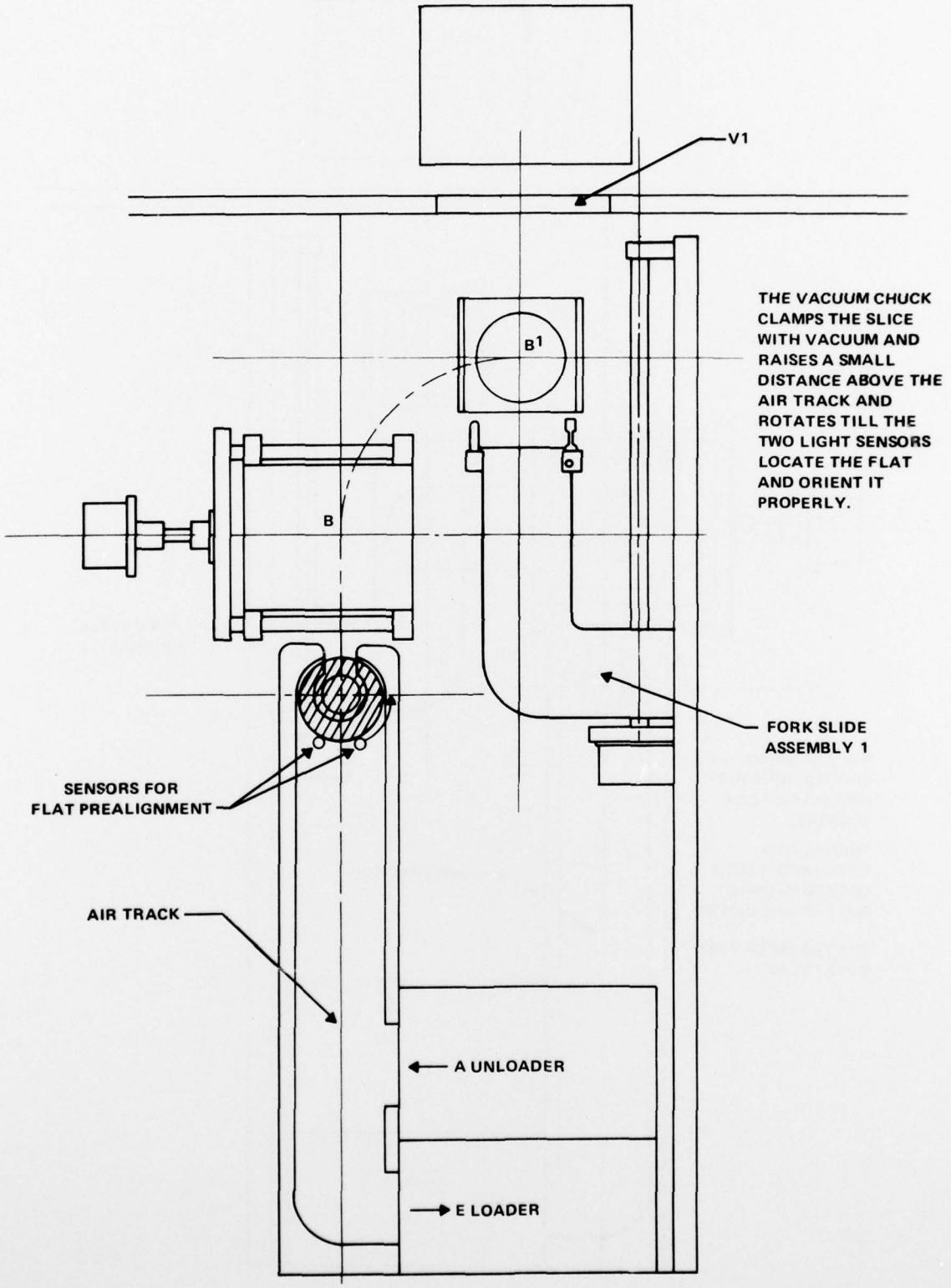

Figure 27. Loader and Prealign Assembly

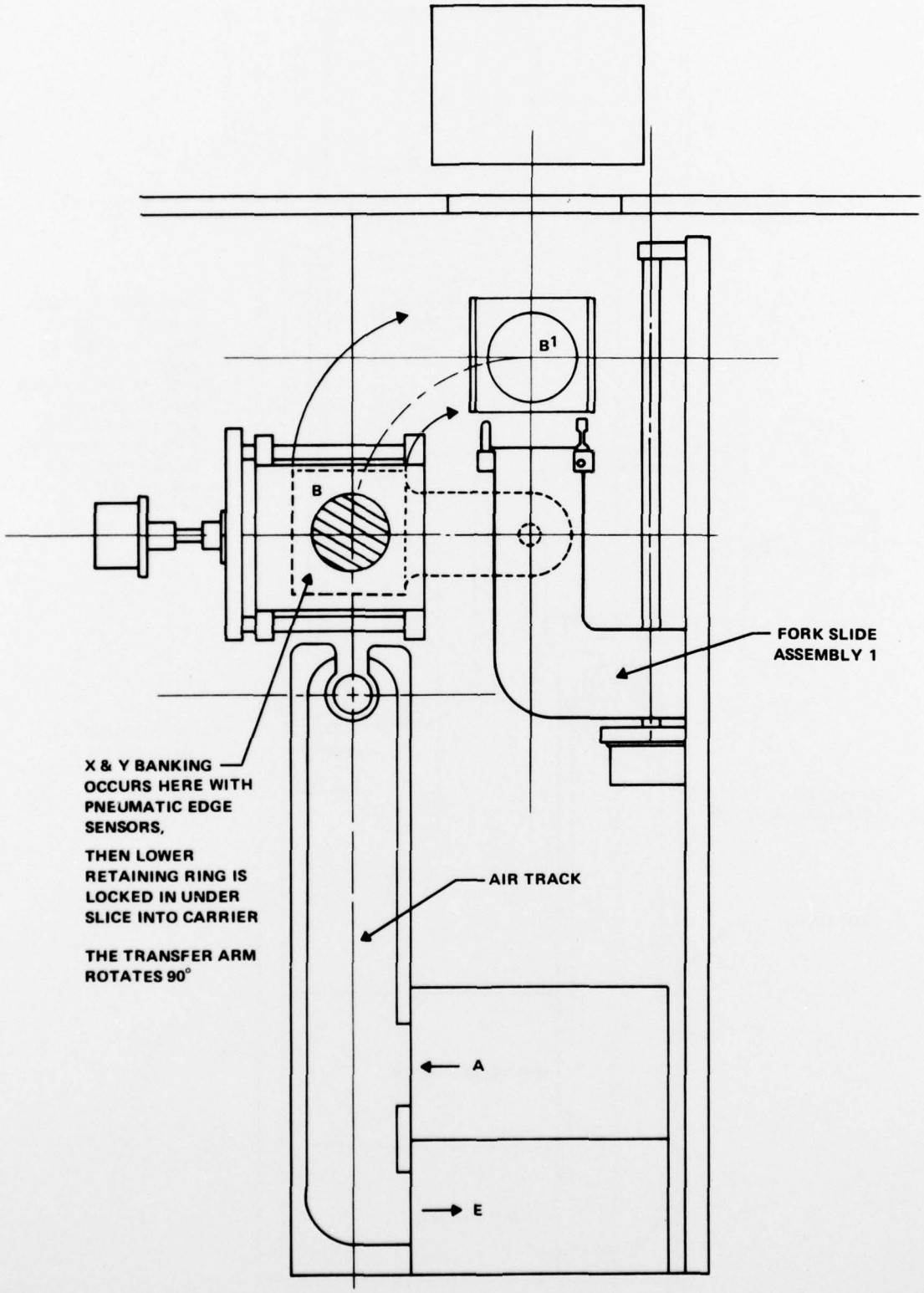

Figure 28. Loader and Prealign Assembly

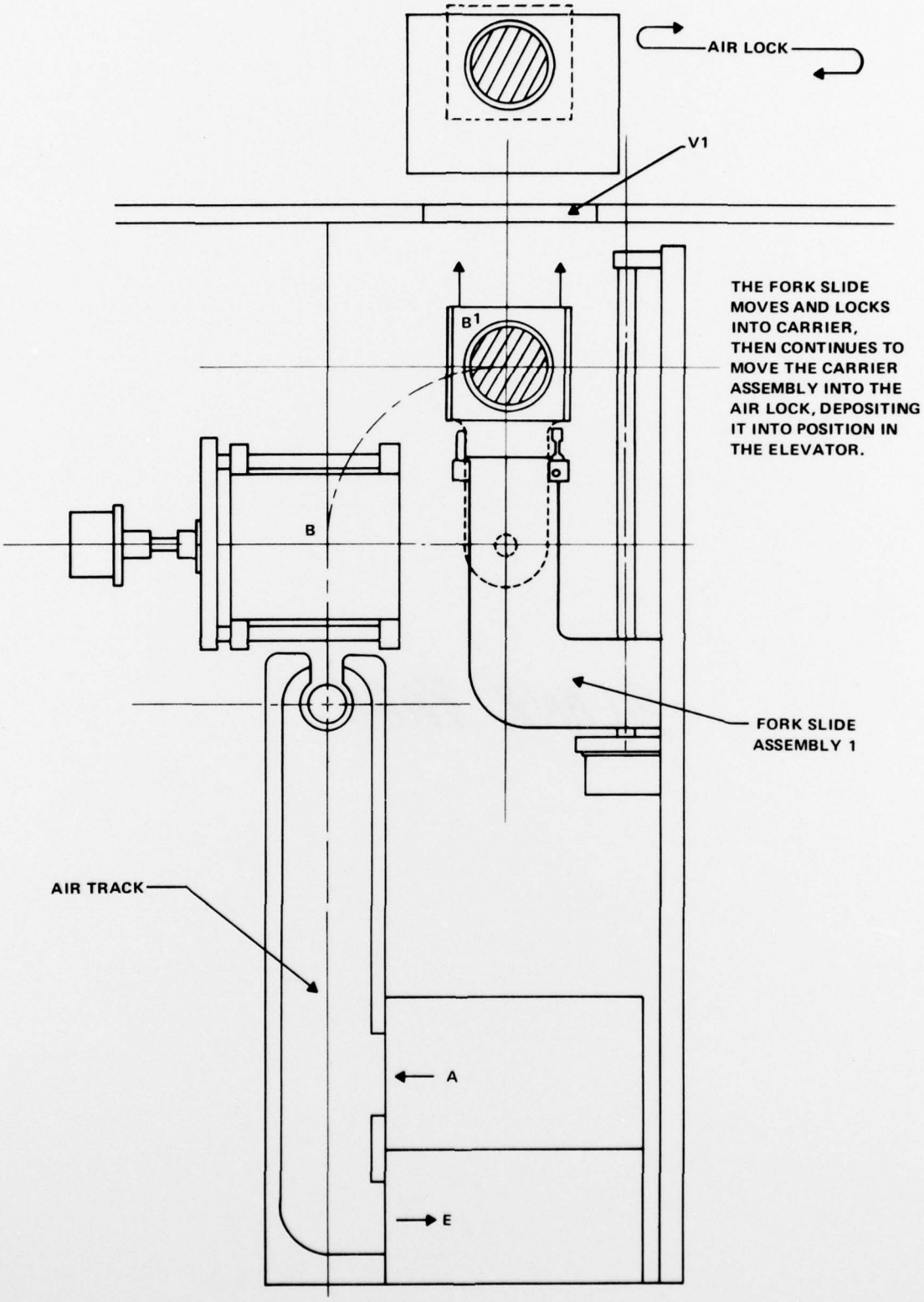

Figure 29. Loader and Prealign Assembly

SECTION III
MANPOWER

The following professionals worked on this program 1 March 1977 – 1 June 1977. The percentage of time worked is also shown.

Mr. P. L. Whelan	50%
Mr. R. A. Williamson	50%
Dr. G. L. Varnell	10%
Dr. J. L. Bartelt	Consultant
Dr. T. L. Brewer	Consultant
Dr. R. J. Dexter	Consultant
Dr. R. A. Robbins	Consultant
Mr. C. D. Winborn	Consultant

In addition, three technicians worked on the program.